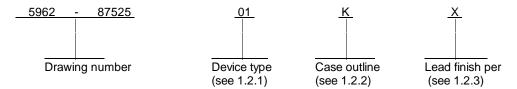
LTR								R	EVISI	ONS			ı							
						ESCF	RIPTIO	N					D.	ATE (Y	'R-MO-[DA)		APPR	OVED)
А	04 ir	Added burn-in condition C to 4.2.a.1 and 4.3.2.b.1. I 04 inactive for new design. Not available from an app Editorial changes throughout.														W. Heckman				
В	Add	Added burn-in condition A to 4.2.a.1 and 4.3.2.b.1.											91-1	1-14			M. Poelking			
С	Add	ed dev	ice typ	es 05 a	and 06	6. Edit	orial ch	nanges	s throu	ıghout.				92-1	2-11			M. Poelking		
	<u> </u>																			
REV																				L
SHEET	C	C																		
SHEET REV	C 15	C 16																		
SHEET REV	15	C 16		REV	<i>J</i>		C	С	C	C	C	C	С	С	С	C	C	C	C	
SHEET REV SHEET	15 US			RE\ SHE			C 1	C 2	C 3	C 4	C 5	C 6	C 7	C 8	C 9	C 10	C 11	C 12	C 13	C 14
SHEET REV SHEET REV STAT	15 US			SHE							5	6	7 SE EL	8 ECTR	9 ONICS	10 S SUP	11 PLY C		13	
SHEET REV SHEET REV STAT OF SHEET PMIC N/A STAN MI	US S DARI	16 DIZE	D	SHE PREI Tir	EET PAREI	oh BY				4	5 D	6 EFENS	7 SE EL DA	8 ECTR AYTON	9 ONICS	10 S SUP IO 454	11 PLY 0	12 CENTE	13 R	1.
SHEET REV SHEET REV STAT OF SHEET PMIC N/A STAN MI DR THIS DRAW FOR	DARI LITAF RAWIN VING IS A USE BY	DIZE RY NG		SHE PREI Tir CHEI Tir	PAREI m H. N CKED m H. N	BY oh	1			4 MIC WID	5 D ROC E AN	6 EFEN:	7 SE EL DA	8 ECTRAYTON	9 ONIC: N, OHI	10 S SUP IO 454	PLY C	12	13 FR	1-
SHEET REV SHEET REV STAT OF SHEET PMIC N/A STAN MI DR THIS DRAW FOR	DARI LITAF RAWIN VING IS A USE BY PARTMEI	DIZE RY NG AVAILA ALL NTS OF TH	ABLE E	SHE PREI Tir CHE Tir APPI Wii	PAREI m H. N CKED m H. N ROVEI lliam K	BY oh D BY . Hecki	1	2		4 MIC WID	5 ROC E AN NOLI	IRCUID 10-	7 SE EL DA	8 ECTR AYTOM HIGH E BUS	9 ONIC: N, OHI	10 S SUP IO 454 FORM	11 PPLY 0 444 MANC	12 CENTE	13 IOS 9 STER	1-,
SHEET REV SHEET REV STAT OF SHEET PMIC N/A STAN MI DF THIS DRAW FOR DEF AND AG DEPARTM	DARI LITAF RAWIN VING IS A USE BY PARTMEI	DIZE RY NG AVAILA ALL NTS OF TH	ABLE E	SHE PREI Tir CHEI Tir APPI Wil	PAREI m H. N CKED m H. N ROVEI Iliam K	BY oh D BY . Hecki	man OVAL [12-02	2		MIC WID MON	5 ROC E AN NOLI	IRCU ID 10- THIC	7 SE EL DA ITS, H -WIDI SILIC	BECTRAYTON	9 ONIC: N, OHI	10 S SUP IO 454 FORM	11 PPLY 0 444 MANC	12 CENTE	13 IOS 9 STER	1-,,

1. SCOPE

- 1.1 <u>Scope</u>. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".
 - 1.2 Part or Identifying Number. The complete PIN shall be as shown in the following example:



1.2.1 <u>Device type(s)</u>. The device type(s) shall identify the circuit function as follows:

Device type	Generic number	<u>Circuit function</u>
01	29C821	High performance CMOS 10-wide bus interface register
02	29C823	High performance CMOS 9-wide bus interface register
03	29C921	High performance CMOS 10-wide bus interface register (rotated die) 1/
04	29C921	High performance CMOS 9-wide bus interface register (rotated die) 1/
05	29C821A	High performance CMOS 10-wide bus interface register (edge-rate controlled outputs)
06	29C823A	High performance CMOS 9-wide bus interface register (edge-rate controlled outputs)

1.2.2 <u>Case outline(s)</u>. The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	<u>Terminals</u>	Package style
K	GDFP2-F24 or GDFP3-F24	24	flat package
L	GDIP3-T24 or CDIP2-T24	24	dual-in-line package
3	CQCC1-N28	28	square leadless-chip-carrier

1.2.5 <u>Lead finish</u>. The lead finish shall be as specified in MIL-M-38510. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ Not available from an approved source of supply.

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1.3 Absolute maximum ratings. Supply voltage range (V_{CC}) -0.5 V dc to +6.0 V dc Storage temperature range -65°C to +150°C DC input voltage range $-0.5 \text{ V dc to V}_{CC} + 0.5 \text{ V dc}$ -0.5 V dc to +6.0 V dc DC output voltage range -0.5 V dc to V_{CC} + 0.5 V dc -0.5 V dc to +6.0 V dc DC output diode current: Into output +50 mA DC output diode current: Out of output -50 mA DC input diode current: Into output +20 mA DC input diode current: Out of output -20 mA DC output current per pin (I_{sink}) +48 mA (2 x IOI) +100 mA

DC output current per pin (I_{source})

-100 mA (n x I_{OL} + m x I_{CCT}) mA $\underline{1}$ / Total dc ground current Total dc V_{CC current}

-30 mA (2 x I_{OL})

+300° C

Thermal resistance, junction-to-case (Θ_{JC}):

Cases L, K and 3 See MIL-STD-1835

Junction temperature (T,J) +150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) +4.5 V dc to +5.5 V dc -55°C to +125°C 2.0 V dc Maximum low level input voltage (V_{IL}) 0.8 V dc

²/ For $T_A = +100^{\circ}$ C to $+125^{\circ}$ C derate linearly at 10mW/ $^{\circ}$ C.

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^{1/} n = number of outputs, m = number of inputs.

2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, bulletin, and bulletin</u>. Unless otherwise specified, the following specifications, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specifications, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

- 3.1 <u>Item requirements</u>. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.
- 3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 herein.
 - 3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.
 - 3.2.2 <u>Terminal connections</u>. The terminal connections shall be as specified on figure 1.
 - 3.2.3 Truth table. The truth table shall be as specified on figure 2.
 - 3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.
- 3.3 <u>Electrical performance characteristics and postirradiation parameter limits</u>. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.
- 3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.
- 3.5 <u>Marking</u>. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).
- 3.6 <u>Certificate of compliance</u>. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 and the requirements herein.
- 3.7 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE I. <u>Electrical performance characteristics</u>.

Test	Symbol	-55°C ≤ T _C ≤ +125°C			Device type	Limit	Unit	
		4.5 V ≤ V ₀	4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified			Min	Max	
High level output voltage	V _{OH}	$V_{CC} = 4.5 \text{ V}, I_{OH}$ $V_{IN} = V_{IL}, V_{IH}$	$V_{CC} = 4.5 \text{ V}, I_{OH} = -15.0 \text{ mA}$ $V_{IN} = V_{IL}, V_{IH}$		All	2.4		V
Low level output	V _{OL}	$V_{CC} = 4.5 \text{ V},$	I _{OL} = 24.0 mA	1, 2, 3	01-04		0.5	V
voltage		$V_{IN} = V_{IL}, V_{IH}$	I _{OH} = 32.0 mA		05,06		0.5	V
Input clamp voltage	V _{IC}	$V_{CC} = 4.5 \text{ V}, I_{IN} =$	-18 mA	1, 2, 3	All		-1.2	V
Low level input	IIL1	V _{CC} = 5.5 V	V _{IN} = 0 V	1, 2, 3	01-04		-10	μ A
current					05,06		-5	μ A
	I _{IL2}		V _{IN} = 0.4 V		01-04		5	μ A
High level input	I _{IH1}	V _{CC} = 5.5 V	V _{IN} = 2.7 V	1, 2, 3	01-04		5	μ A
current	I _{IH2}]	V _{IN} = 5.5 V		01-04		10	μ A
					05,06		5	μ A
Off state current	I _{OZH}	V _{CC} = 5.5 V	V _{OUT} = 5.5 V	1, 2, 3	All		10	μ A
	I _{OZL}		V _{OUT} = 0.0 V	1, 2, 3	All		-10	μ A
Output short circuit current	I _{SC}	V _{CC} = 5.5 V, V _{OL}	_{JT} = 0 V <u>1</u> /	1, 2, 3	aLL	-60		mA
Static supply	I _{CCQ}	$V_{CC} = 5.5 \text{ V},$	$V_{CC} = 5.5 \text{ V or}$	1, 2, 3	01-04		160	μ A
current		outputs open	GND		05,06		1500	μ A

See footnotes at end of table.

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		TABLE I. Elec	ctrical per	formance chara	acteristics - Con	tinued.			
Test	Symbol	Test conditions -55° C ≤ T _C ≤ +125° C		Group A subgroups	Device type	Limits 2/		Unit	
		4.5 V	′ ≤ V _{CC} ≤ otherwise	5.5 V		,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	Min	Max	
Static supply	I _{CCT}	VCC =5.5 V,	V _{IN} = 3	.4 V		All		1.5	mA/bit
current		Outputs open	Data input	OE, CP		01,03 05		3.0	
				OE, EN CLR, CP		02,04,06		3.0	
Input capacitance	C _{IN}	See 4.3.1c			4	All		16	pF
Output capacitance	C _{OUT}	See 4.3.1c			4	All		20	pF
Functional testing		See 4.3.1d			7,8	All			
Propagation delay	t _{PLH}	See figure 4			9,10,11	01-04		14	ns
clock (CP) to Y _I		C _L = 50 pF F	R ₁ = 5000	Ω		05,06		9.5	ns
Propagation delay	t _{PHL}	R	$R_2 = 500\Omega$			01-04		14	ns
clock (CP) to Y						05,06		9.5	ns
Propagation delay	t _{PHL}				9,10,11	01-04		15	ns
clear to Y _I						05,06		10.5	ns
Propagation delay output enable	t _{PZH}				9,10,11	01-04		14	ns
(OE) to Y _I						05,06		9	ns
Propagation delay output enable	t _{PZL}				9,10,11	01-04		14	ns
(OE) to Y _I						05,06		13	ns

See footnotes at end of table.

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Test	Symbol	Conditions -55° C ≤ T _C ≤ +125° C	Group A subgroups	Device type	Lim	Unit	
		$4.5 \text{ V} \leq \text{V}_{CC} \leq 5.5 \text{ V}$ unless otherwise specified			Min	Max	
Propagation delay output disable		See figure 4	9,10,11	01-04		14	ns
(OE) to Y _I		$CL = 50 \text{ pF R}_1 = 500\Omega$		05,06		8.5	ns
Propagation delay output disable	t _{PLZ}	$R_2' = 500\Omega$	9,10,11	01-04		14	ns
(OE) to Y _I				05,06		8.5	ns
Data (D _I) to CP	t _s		9,10,11	01-04	6		ns
setup time				05,06	3		ns
Data (D _I) to CP hold time	t _H		9,10,11	01-04	3		ns
noid time				05,06	2		ns
Enable (high to	t _s		9,10,11	01-04	6		ns
low) to CP setup				05,06	4		ns
Enable (low to	t _s		9,10,11	01-04	6		ns
high) to CP setup				05,06	4		ns
Enable hold time	t _H		9,10,11	01-04	3		ns
				05,06	0		ns
Clear (low to high)	t _s		9,10,11	01-04	6		ns
to CP setup time	t _{REC}			05,06	6		ns
Clock low pulse	t _{PWL}		9,10,11	01-04	11		ns
width				05,06	6		ns

See footnotes at end of table.

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TABLE I. <u>Electrical performance characteristics</u> - continued.

Test	Symbol	Conditions -55° C ≤ T _C ≤ +125° C	Group A subgroups	Device type	Lim	nits	Unit
		$4.5~V \le V_{CC} \le 5.5~V$ unless otherwise specified			Min	Max	
Clock high pulse	t _{PWH}		9,10,11	01-04	11		ns
				05,06	6		ns
Clear pulse width	t _{PWL}		9,10,11	01-04	11		ns
				05,06	6		ns

1/ Not more than one output shorted at a time. Duration should not exceed 100 miliseconds.

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Device types 01 and 05 Device types 01 and 05 Case 3 Cases K and L ŌĒ ☐ 1 ● 24 \ V_{CC} D_1 D_0 \overline{OE} NC V_{CC} Y_0 Y_1 $D_0 \square 2$ 23 Y₀ 22 X Y₁ 4 3 2 **1** 28 27 26 D₂ \(\sqrt{5} \) 25 🖂 Y₂ 21 Y₂ D3 7 6 24 🖂 Y₃ 20 \ Y₃ D₄ \(\square 7 23 □ Y₄ 19 Y₄ NC > 8 22 🖂 NC D₅ \(\square 9 21 ☐ Y₅ 18 Y Y 5 20 ⊏ Y₆ D₆ \(\square 10 17 Y₆ D₇ \(\square 11 19 ☐ Y₇ D₇ 🛮 9 16 Y₇ 12 13 14 15 16 17 18 D₈ [10 15 Y₈ D₈ D₉ GND NC CP Y₉ Y₈ D₉ [11 14 \ Yq GND [12 13 CP Device types 02 and 06 Device types 02 and 06 Cases K and L Case 3 ŌĒ ☐ 1 ● 24 V CC D_1 D_0 $\overline{\mathsf{OE}}$ NC V_CC Y_0 Y_1 $D_0 \square 2$ 23 Y₀ YYYYYYY 4 3 2 **1** 28 27 26 $D_1 \square 3$ 22 Y₁ D₂ 5 25 🗖 Y₂ 21 Y₂ D₃ \(\sigma \) 6 24 🖂 Y₃ D₃ 5 20 Y Y 3 D₄ \(\sum 7 23 □ Y₄ 19 Y4 NC > 8 22 🗖 NC 18 Y₅ D₅ \(\sigma 9 21 ☐ Y₅ D₆ \(\square 10 20 ⊏ Y₆ 17 Y Y6 D₇ \(\square 11 19 ⊏ Y₇ D₇ 9 16 Y₇ 12 13 14 15 16 17 18 D₈ [10 15 Y₈ 14 EN D₈ CLR GND NC CP EN Y₈ CLR [11

FIGURE 1. Terminal connections.

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GND 🗌 12

13 CP

Device type 03 Device type 04 Case L Case L Y 4 Y₅ Y 4 Y 5 24 24 1 🚳 23 Y 3 23 Y 3 Y₆ 2 2 Y 2 Y₂ Y 7 3 22 Y 7 3 22 Y ₁ Y₈ Y ₁ 21 21 Y 0 Yn 20 5 5 20 Υq ΕN $^{\rm V}$ C C [∨]cc ☐ 6 19 СР 19 СР 6 ŌΕ ŌΕ 18 🗍 GND 18 GND D_0 D₀ D₉ 17 8 17 CLR D_1 D_1 16 16 Da 9 D_8 9 D₂ D_2 $15 \square D_7$ D₇ 10 15 10 D3 D_3 14 D₆ 11 14 D₆ 11 D₄ D₄ D₅ 12 13 D₅ 12 13 FIGURE 1. <u>Terminal connections</u> - continued.

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Device types 01, 03, and 05

I	nputs	3	Internal	Outputs	
ŌE	Di	СР	Qi	Yi	Function
H	L	†	H	Z	Hi-Z
H	H	†	L	Z	
L	L	†	H	L	Load
L	H	†	L	H	

Device types 02, 04, and 06

	Inputs			Internal	Outputs		
							Function
ŌE	CLR	EN	D _i	СР	Q _i	Yi	
H	ΗH		L H	1	H L	Z Z	Hi-Z
П	П	L	П	- 1	L		
Н	L	Χ	Х	Х	Н	Z	Clear
L	L	Χ	Χ	Х	Н	L	
Н	Н	Н	Х	Χ	NC	Z	Hold
L	Н	Н	X	Х	NC	NC	
Н	Н	L	L	1	Н	Z	
Н	Н	L	Н	1	L	Z Z	Load
L	Н	L	L	1	Н	L	
L	Н	L	Н	1	L	Н	

H = high L = Low X = Don't care

FIGURE 2. Truth Table.

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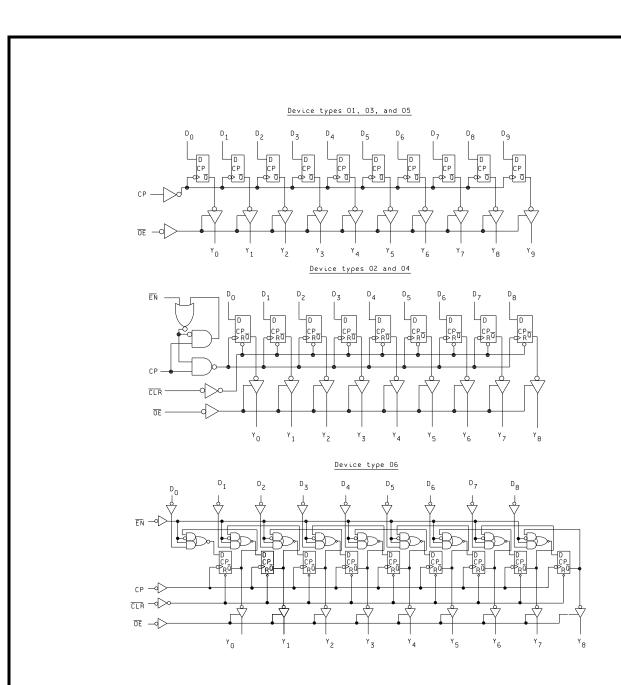
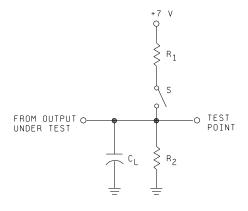


FIGURE 3. Logic diagrams.

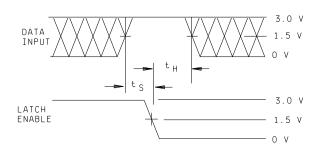
STANDARDIZED MILITARY DRAWING	SIZE A		5962-88516
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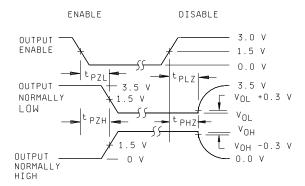
Parameter	S Position
t _{PLH}	Open
t _{PHL}	Open
^t PHZ	Open
t _{PZH}	Open
t _{PLZ}	Closed
^t PZL	Closed

Load circuit for three-state outputs

Setup and hold times



Enable and disable times



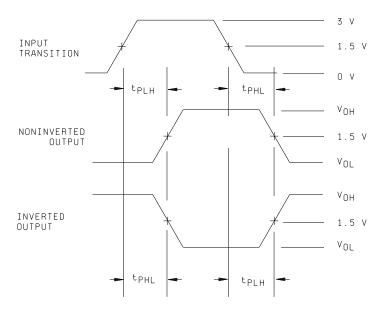
NOTES:

- 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
- 2. Cross hatched area is don't care condition.

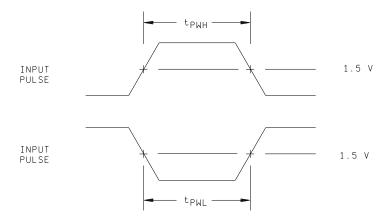
FIGURE 4. Test circuit and switching waveforms.

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Propagation delay



Pulse width



NOTE: Pulse generator for all pulses rate $_{\leq}$ 1.0 Mhz; Z $_{0}$ = 500 $\Omega;$ t_{r} $_{\leq}$ 2.5 ns; t_{f} $_{\leq}$ 2.5 ns.

FIGURE 4. <u>Test circuit and switching waveforms</u> - cotinued.

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- 3.8 <u>Notification of change</u>. Notification of change to DESC-ec shall be required in accordance with MIL-STD-883 (see 3.1 herein)
- 3.9 <u>Verfication and review</u>. DESC, DESC's agent, and acquiring activity retain the option to review the manufactrer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.
 - 4. QUALITY ASSURANCE PROVISIONS
- 4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).
- 4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:
 - a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the requirements for inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ} C$, minimum.
 - b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.
- 4.3 <u>Quality conformance inspection</u>. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.
 - 4.3.1 Group A inspection.
 - a. Tests shall be as specified in table II herein.
 - b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
 - Subgroups 4 (C_{IN} and C _{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.
 - d. Subgroups 7 and 8 shall include verification of the truth tables.
 - 4.3.2 Group Cand D inspections.
 - a. End-point electrical parameters shall be as specified in table II herein.
 - b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the requirements for inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ} C$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5004)	1, 2, 3, 7, 8, 9, 10, 11
Group C and D end-point electrical parameters (method 5005)	1, 2, 3

^{*} PDA applies to subgroups 1 and 7.

- 5. PACKAGING
- 5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.
- 6. NOTES
- 6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for original equipment manufacturer application. When a military specification exists and the product covered by this drawing has been qualified listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.
- 6.2 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.
- 6.3 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).
- 6.4 <u>Record of users</u>. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.
- 6.5 <u>Comments</u>. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.
- 6.6 <u>Approved sources of supply</u>. Approved sources of supply is listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED		
MILITARY DRAWING		
DEFENSE ELECTRONICS SUPPLY CENTER		
DAYTON, OHIO 45444		

SIZE A		5962-88516
	REVISION LEVEL C	SHEET 16

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 92-12-11

Approved sources of supply for SMD 5962-88516 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN <u>1</u> /
5962-8851601LX	34335	AM29C821/BLA
5962-8851601KX	34335	AM29C821/BKA
5962-88516013X	34335	AM29C821/B3A
5962-8851602LX	34335	AM29C823/BLA
5962-8851602KX	34335	AM29C823/BKA
5962-88516023X	34335	AM29C823/B3A
5962-8851603LX	<u>2</u> /	AM29C921/BLA
5962-8851604LX	<u>2</u> /	AM29C923/BLA
5962-8851605LX	34335	AM29C821A/BLA
5962-8851605KX	34335	AM29C821A/BKA
5962-88516053X	34335	AM29C821A/B3A
5962-8851606LX	34335	AM29C823A/BLA
5962-8851606KX	34335	AM29C823A/BKA
5962-88516063X	34335	AM29C823A/B3A

- 1/ <u>Caution</u>. Do not use this number for item acquisition. Items acquired to this number may not satis fy the performance requirements of this drawing.
- 2/ Device types 03 and 04 inactive for new design. Not available from an approved source.

Vendor CAGE	Vendor name
<u>number</u>	and address

34335 Advanced Micron Devices, Incorporated 901 Thompson Place P.O. Box 3453 Sunnyvalve, CA 94088

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.